XFP LC Bi-Directional (BiDi) Optical Transceivers

INTRODUCTION

This design guide provides the information needed to incorporate OptixCom's fiber optics transceiver products in the customer's system. The BiDi XFP series of transceiver products are compliant with the XFP mutli-source agreement (MSA) INF-8077i (Rev. 4.5, 2005) and IEEE 802.3 Section 4 on "52. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-S (short wavelength serial), 10GBASE-L (long wavelength serial), and 10GBASE-E (extra long wavelength serial)". For more detail information, please refer to the URL http://www.xfpmsa.org or visit OptixCom web site: http://www.OptixCom.com for the official documentation.

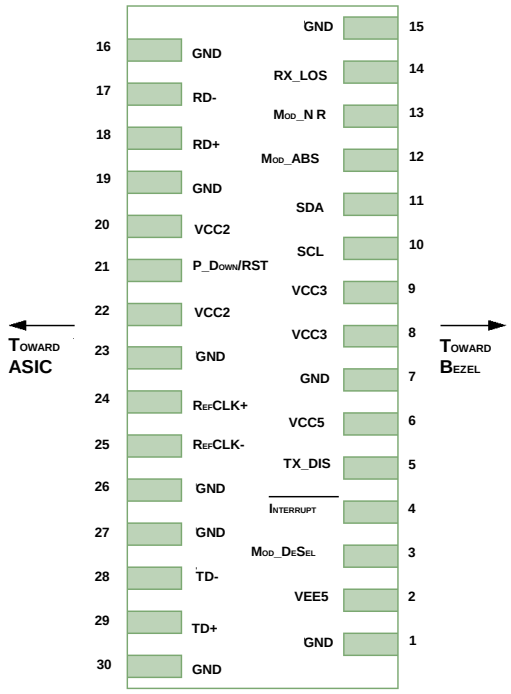
The reference guide covers the following topics:

A. PIN ASSIGNMENT & DESCRIPTION
B. RECOMMENDED INTERFACE CIRCUIT
C. PACKAGE OUTLINE
D. SFP TRANSCEIVER HOST BOARD MECHANICAL LAYOUT
E. ELECTRICAL CONNECTOR MECHANICAL LAYOUT
F. CONNECTOR INSERTION, EXTRACTION, AND RETENTION FORCE
G. TIMING REQUIREMENTS

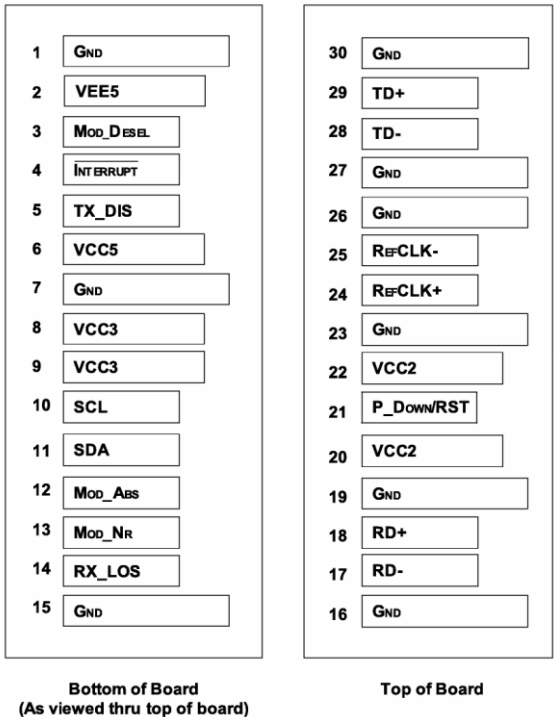
A. PIN ASSIGNMENT & DESCRIPTION

The XFP transceiver contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating in the following order: ground contacts, power contacts, and signal contacts.

Host Board Connector Pad Layout



XFP Transceiver Pad Layout



Bottom of Board
(As viewed thru top of board)

Top of Board

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Pin	Logic	Symbol	Name/Description	Note
1		GND	Module Ground	1
2		VEE5	Optional -5.2V Power Supply	
3	LVTTL-I	Mod_DeSel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	Interrupt	Interrupt; Indicates presence of an important condition which can be read over the 2-wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	2-Wire Serial Interface Clock	2
11	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply	3
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode.	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board	
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board	
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins Gnd are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3. 15V and 3.45V on the host board.
3. The 1.8 V power supply can be optionally programmed to voltages lower than 1.8 V in modules supporting the variable power supply.

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LOW SPEED ELECTRICAL HARDWARE PINS

In addition to the 2-wire serial interface the XFP module has the following low speed pins for control and status:

Mod_NR	Mod_DeSel	Interrupt	TX_DIS
Mod _ABS	RX_LOS	P_Down/RST.	

MOD_NR

The Mod_NR is an output pin that when High, indicates that the module has detected a condition that renders transmitter and or receiver data in-valid, shall consist of logical OR of the following signals:

- Transmit Signal Conditioner Loss of Lock
- Transmitter Laser Fault
- Receiver Signal Conditioner Loss of Lock

Other conditions deemed valuable to the detection of fault may be added to the Mod_NR. The Mod_NR output pin is an open collector and must be pulled to Host_Vcc on the host board.

MOD_DESEL

The Mod_DeSel is an input pin. When held Low by the host, the module responds to 2-wire serial communication commands. The Mod_DeSel allows the use of multiple XFP modules on a single 2-wire interface bus. When the Mod_DeSel pin is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. Mod_DeSel pin must be pulled to VCC3 in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire inter-face communications within the Mod_DeSel assert time after any XFP modules are deselected. Similarly, the host must wait at least for the pe-riod of the Mod_DeSel deassert time before communicating with the newly selected module. The assertion and de-assertion periods of dif-ferent modules may overlap as long as the above timing requirements are met.

INTERRUPT

Interrupt is an output pin. When "Low", indicates possible module opera-tional fault or a status critical to the host system. The Interrupt pin is an open collector output and must be pulled up to Host_Vcc the host board.

TX_DIS

TX_DIS is an input pin. When TX_DIS is asserted High, the XFP module transmitter output must be turned off. The TX_DIS pin must be pulled up to VCC3 in the XFP module.

MOD_ABS

Mod_ABS is pulled up to Host_Vcc on the host board and grounded in the XFP module. Mod_ABS is then asserted "High" when the XFP module is physically absent from a host slot.

RX_LOS

The RX_LOS when High indicates insufficient optical power for reliable signal reception. The RX_LOS pin is an open collector output and must be pulled up to Host_Vcc on the host board.

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P_DOWN/RST

This is a multifunction pin for module Power Down and Reset. The P_Down/RST pin must be pulled up to VCC3 in the XFP module.

POWER DOWN FUNCTION

The P_Down pin, when held High by the host, places the module in the standby (Low Power) mode with a maximum power dissipation of 1.5W. This protects hosts which are not capable of cooling higher power mod-ules which may be accidentally inserted.

The module's 2-wire serial interface and all laser safety functions must be fully functional in this low power mode. During P_Down, the module shall still support the completion of reset Interrupt, as well as maintain function-ality of the variable power supply.

RESET FUNCTION

The negative edge of P_Down/RST signal initiates a complete module reset.

MODULE BEHAVIOR DURING POWER DOWN AND RESET

During execution of a reset (t_init) or while held in Power Down mode, a module may be unable to determine the correct value for Mod_NR and RX_LOS. These outputs as well as all interrupt related flags, except com-pletion of Reset flag, shall be disregarded by the host. When the module completes a Reset and is not in Power Down mode, the module must rep-resent the correct value of both signals on its outputs before posting a completion of reset interrupt to the host.

At no time shall a module cause spurious assertion of the Interrupt pin.
When a host initially applies power to a module with the P_Down/RST signal asserted, a module comes up in power down mode. The module shall only assert the Interrupt signal pin to inform the host it has completed a reset. The completion of reset flag shall be the only interrupt source flag set during power down mode. The host is expected to clear this interrupt before releasing the module from the power down mode. The transition from power down mode to normal mode will trigger a reset of the module and result in a 2nd module reset and a 2nd reset completion interrupt to the host

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LOW SPEED ELECTRICAL SPECIFICATIONS

Low speed signaling is based on Low Voltage TTL (LVTTL) operating at Vcc3 at a nominal supply of (3.3V± 5%). Hosts shall use a pull-up resistor connected to a host_Vcc of +3.3 volts (3.15 to 3.45 volts) on the 2-wire interface SCL (clock), SDA (Data), and all low speed status outputs.

The XFP low speed electrical specifications are given in the following. This specification ensures compatibility between host bus masters and XFP SCL/SDA lines and compatibility with I^2C.

LOW SPEED CONTROL AND SENSE SIGNALS, ELECTRONIC CHARACTERISTICS

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
XFP Interrupt, Mod_NR, RX_LOS	V_{OL}	0.0	0.40	V	Rpullup pulled to host_Vcc, measured at host side of connector. I_{OL}(max) = 3 mA
	V_{OH}	host_Vcc - 0.5	host_Vcc + 0.3	V	Rpullup pulled to host_Vcc, measured at host side of connector.
XFP TX_Dis, P_Down/RST	V_{IL}	-0.3	0.8	V	Rpullup pulled to VCC3,measured at XFP side of connector. I_{IL}(max) = -10 uA
	V_{IH}	2.0	VCC3 + 0.3	V	Rpullup pulled to VCC3, measured at XFP side of connector. I_{IH}(max) = 10 uA
XFP SCL and SDA	V_{OL}	0.0	0.40	V	Rpullup[1] pulled to host_Vcc, measured at host side of connector. I_{OL}(max) = 3 mA
	V_{OH}	host_Vcc - 0.5	host_Vcc + 0.3	V	Rpullup[1] pulled to host_Vcc, measured at host side of connector.
XFP SCL and SDA	V_{IL}	-0.3	Vcc3*0.3	V	Rpullup[1] pulled to Host_VCC, measured at XFP side of connector. I_{IL}(max) = -10 uA
	V_{IH}	Vcc3*0.7	VCC3 + 0.5	V	Rpullup[1] pulled to Host_VCC, measured at XFP side of connector. I_{IH}(max) = 10 uA
Leakage Current	I_I	-10	10	µA	
Capacitance for XFP SCL and SDA I/O Pin	C_i		14	pF	10pF for XFP IC I/O pin, 4 pF for XFP PCB trace
Total bus capacitive load for SCL and for SDA	C_b		100	pF	At 400 KHz, 3.0 Kohms Rp, max At 100 KHz, 8.0 Kohms Rp, max
			400	pF	At 400 KHz, 0.80 Kohms Rp, max At 100 KHz, 2.0 Kohms Rp, max

1. For combinations of Rpullup (Rp), bus capacitance and speed, see Philips I^2C specification revision 2.1, figures 39 and 44. Rise and fall time measurement levels are defined in the XFP management interface ac electrical specifications. Active bus termination may be used by the host in place of a pullup resistor, as described in the Philips I2C specification

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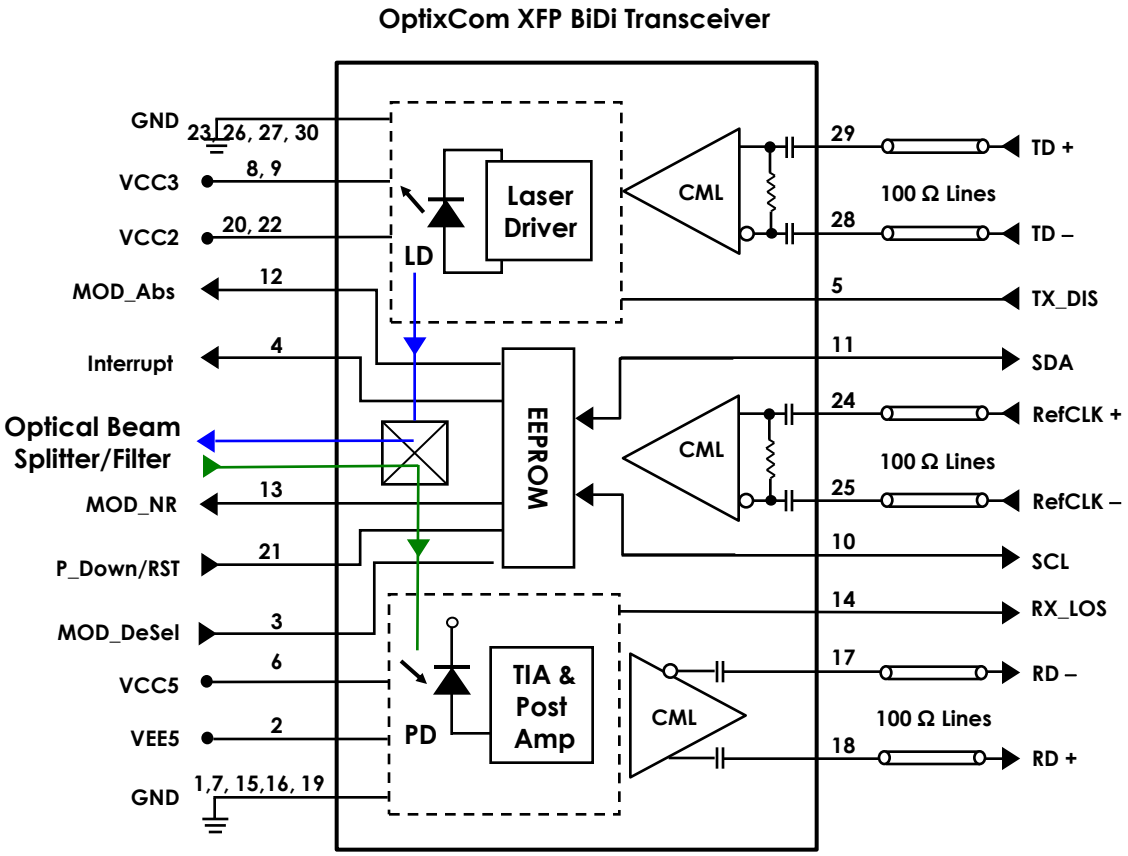
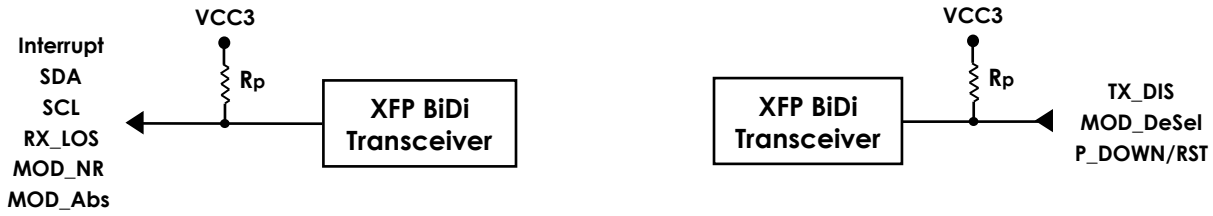
B. RECOMMENDED INTERFACE CIRCUIT



All the LVTTL interface logic pins are open collector compatible. A pull up resistor R_P is used in the following scheme. The value of R_P is between 4.7KΩ to 10K Ω.



The XFP host has 3 power supplies +1.8 V, +3.3 V, +5.0 V and an optional -5.2 V supply. The +1.8 V and +3.3 V supplies have two designated power pins in the connector for each power supply rail. The +5 V and -5.2 sup-plies have one designated power pin each. The maximum continuous or peak current carrying capacity for each connector pin is 500 mA.

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The host system may alter the VCC2 supply to a voltage level lower that the nominal +1.8 V value. This mode of operation is optional and can be supported by modules and hosts that strive to meet lower power/current requirements. Modules supporting this optional lower power mode must be backwards compatible with modules and hosts supporting only 1.8 V on VCC2, i.e. modules implementing these optional modes must be able to operate normally with a voltage of +1.8 V applied on their VCC2 pins (albeit with higher power dissipation). XFP module maximum power dissipation must meet one of the following classes:

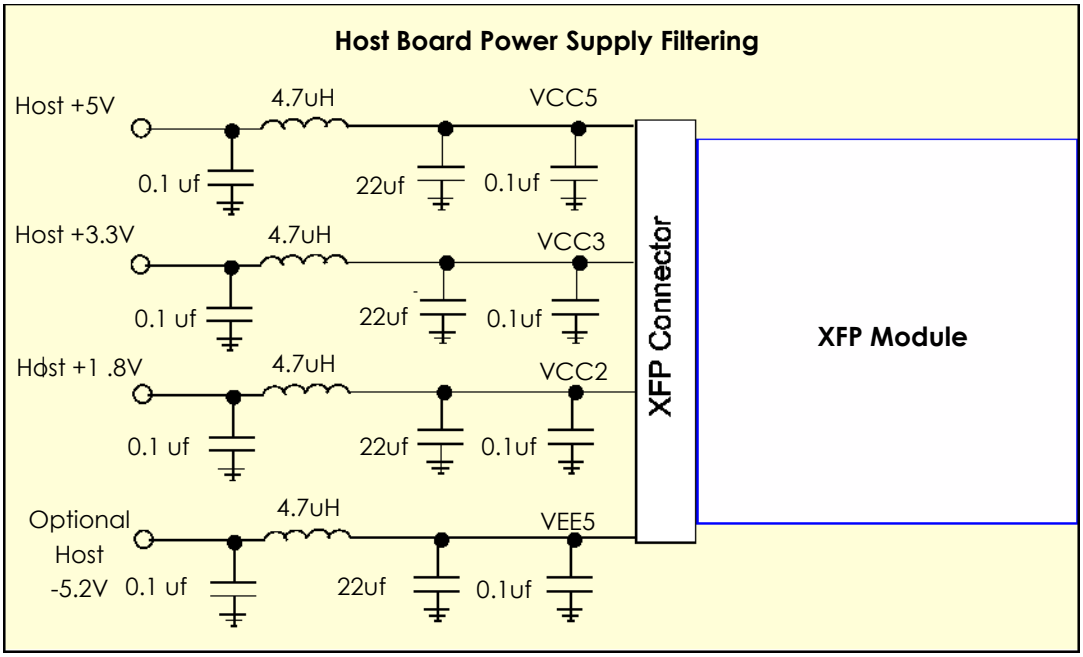
Power Level 1 modules – Up to 1.5 W
Power Level 2 modules – Up to 2.5 W
Power Level 3 modules – Up to 3.5 W
Power Level 4 modules – Greater than 3.5 W

To avoid exceeding system power supply limits and cooling capacity, the module may be placed in the power down mode by pulling pin 21 High. This guarantees module operating in Low Power mode with maximum power dissipation of ≤ 1.5W.

A host board together with XFP module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host and limits inrush charge/current during hot plug insertion.

The example host board power supply filtering shown below will meet the noise filtering requirements in most systems. Other filtering implementations or local regulation may be used to meet the power noise output requirements described in Section 2.7.1 of XFP MSA document.

Any voltage drop across a filter network on the host is counted against the Host DC set point accuracy specification in Table 4 of XFP MSA . For this reason, the example filter may not be appropriate for a host powering multiple XFPs and/or other host components from a shared voltage supply.



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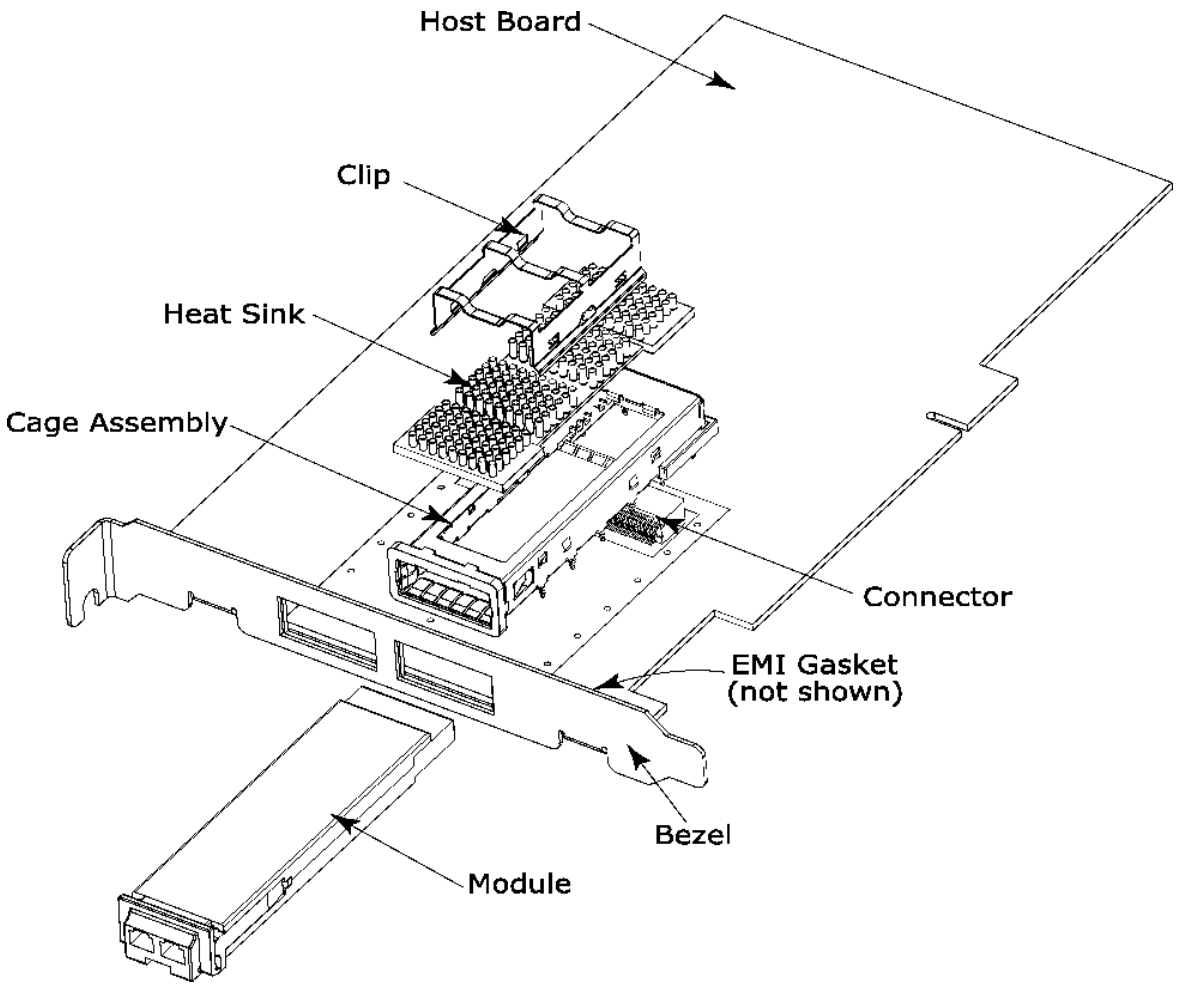
C. PACKAGE OUTLINE

The mechanical components defined in this section are illustrated in the following. The module, clip and connector dimensions are constant for all applications. While the bezel, cage assembly, EMI gasket and heat sink can be designed and/or adjusted for the individual application. The relatively small form factor of the XFP module combined with an adaptable heatsink option allows host system design optimization of module location, heat sink shape/dimension/fins design, and airflow control. The module can be inserted and removed from the cage with the heat sink and clip attached. Please note that OptixCom only offers the XFP transceiver module but not other components. Refer to XFP MSA document for more details of the other components.

XFP Mechanical Components



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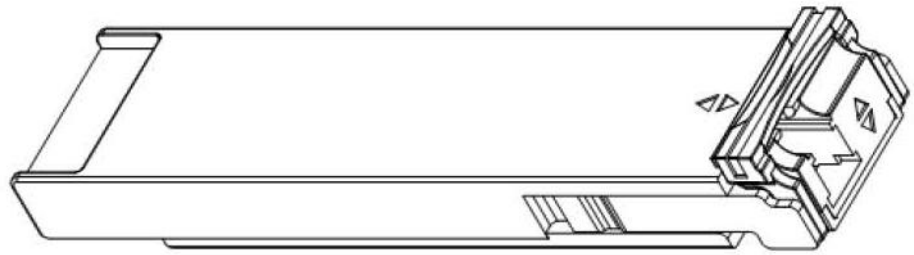
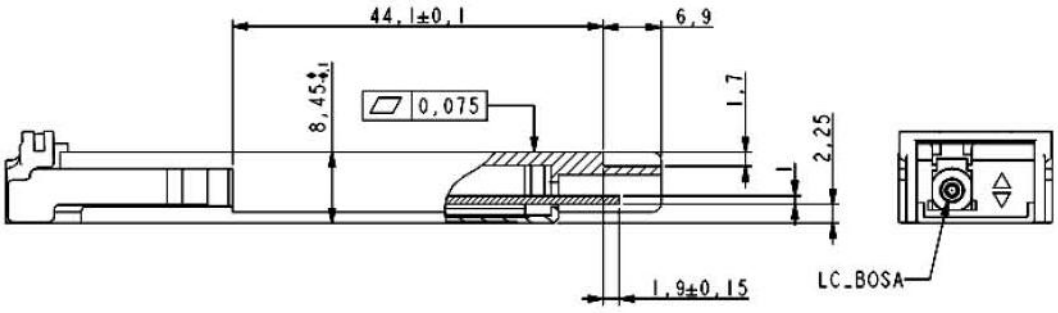
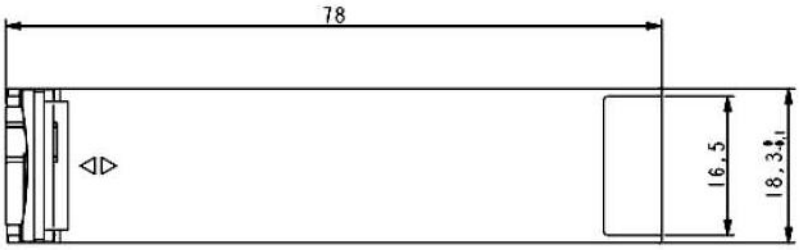
Mechanical Outline Dimensions







Unit: mm, typical tolerance for these dimensions is ± 0.2 mm

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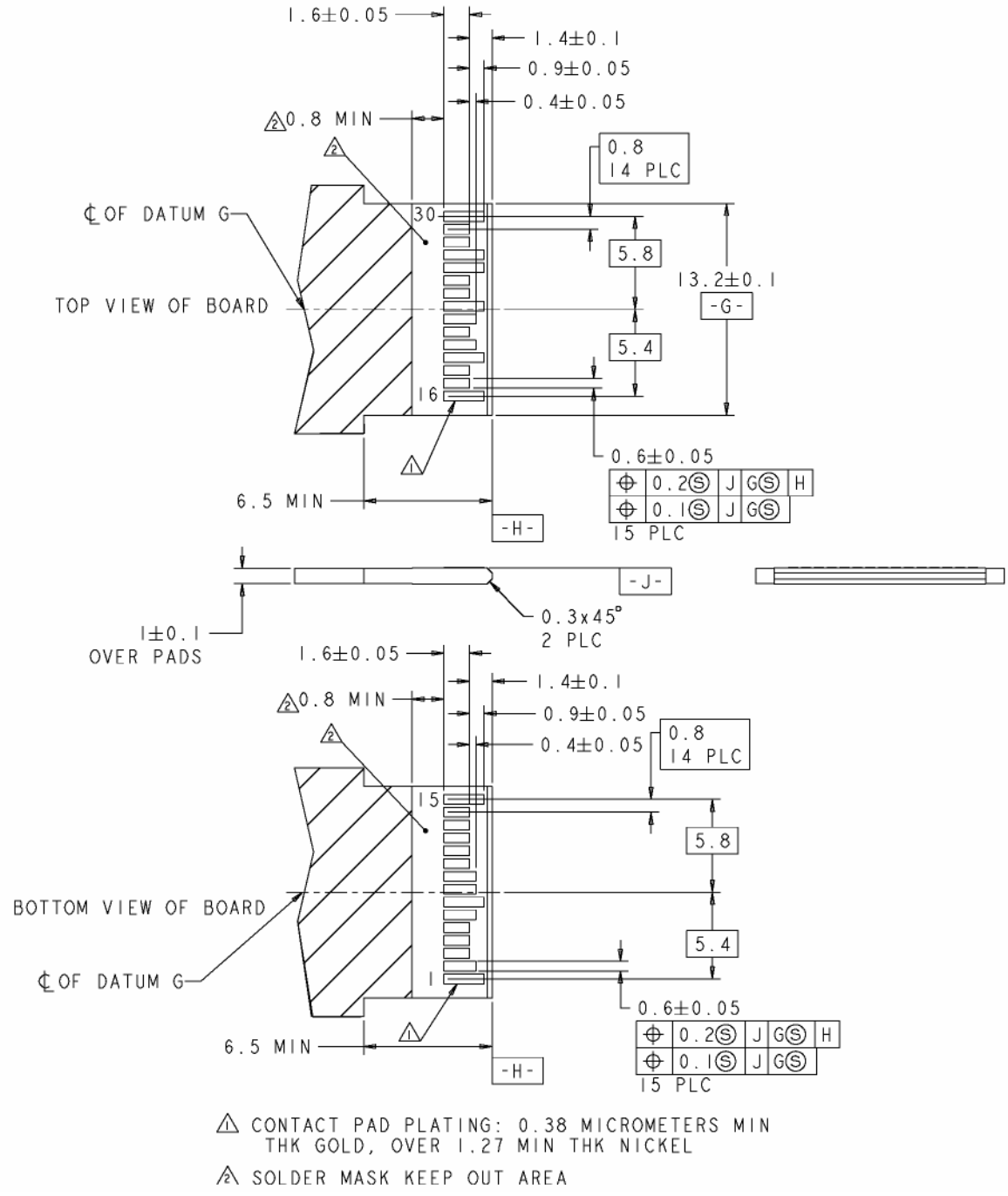
D. XFP TRANSCEIVER HOST BOARD MECHANICAL LAYOUT

The design of the mating portion of the transceiver printed circuit board and the electrical pad layout is illustrated in the following. The recommended contact pad plating for the printed circuit board is 0.38 micrometers minimum gold over 1.27 micrometers minimum thick nickel.



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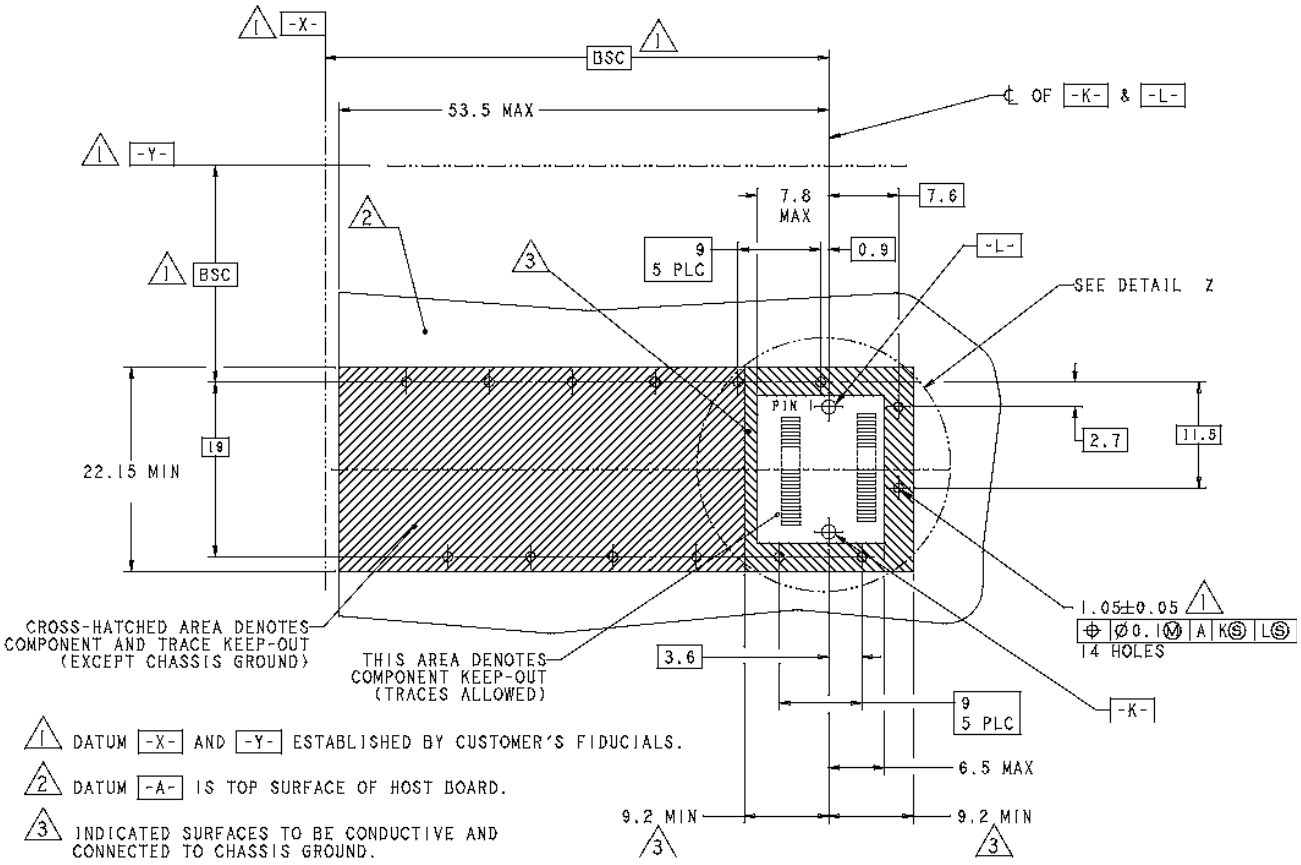

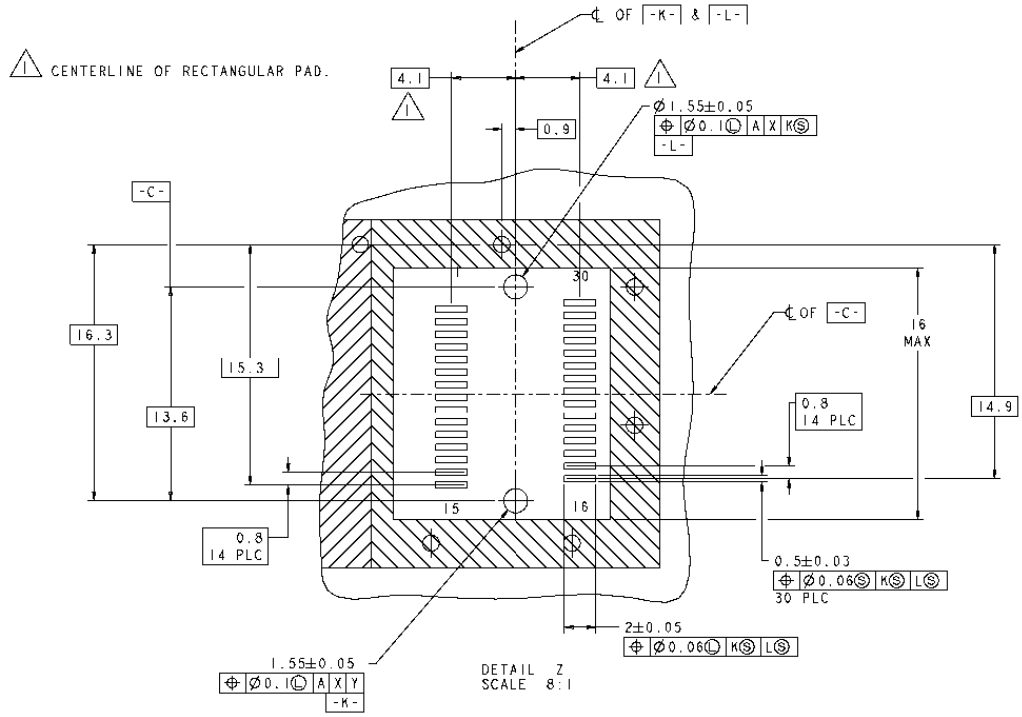

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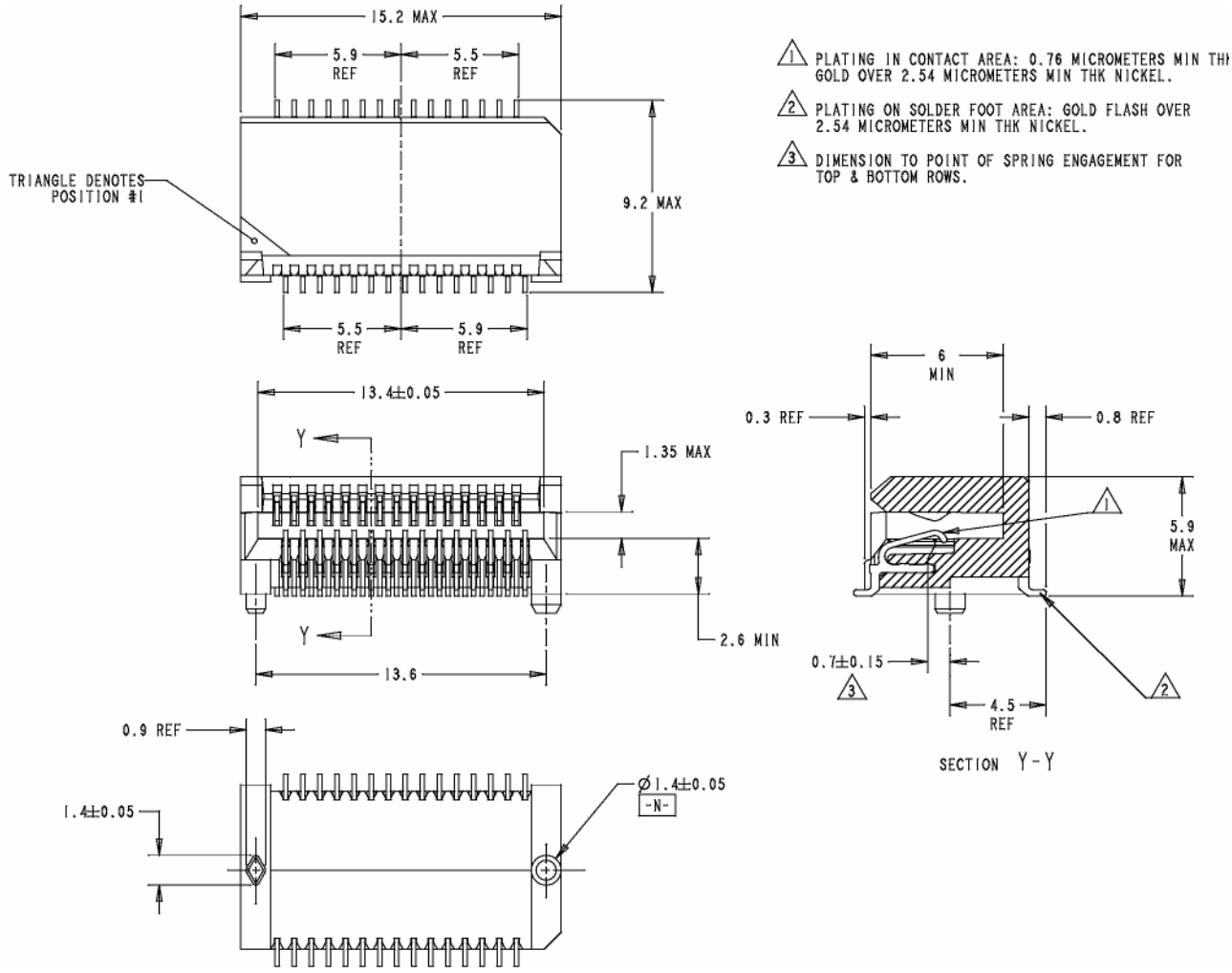
E. ELECTRICAL CONNECTOR MECHANICAL LAYOUT

The XFP Connector is a 30-contact, right angle surface mount connector and available from several manufacturers1. An example connector such as 788862-2 manufactured by Tyco is shown in the following. Newer versions of this connector are available from Tyco, Molex, and Harting with im-proved electrical performance.



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F. CONNECTOR INSERTION, EXTRACTION, AND RETENTION FORCE

The requirement for the various functional forces and the durability cycles are specified in the following Table.

Measurement	*Minimum*	*Maximum*	*Units*	*Comments*
XFP transceiver insertion	0	40	Newtons	
XFP transceiver extraction	0	30	Newtons	
XFP transceiver retention	90	N/A	Newtons	No damage to transceiver below 90N
Cage retention (Latch strength)	180	N/A	Newtons	No damage to the latch below 180N
Cage retention in Host Board	133	N/A	Newtons	Force to be applied in a vertical direction with no damage to the cage.
Insertion / removal cycles, connector/cage	100	N/A	cycles	
Insertion / removal cycles, XFP Transceiver	50	N/A	cycles	

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G. TIMING REQUIREMENTS OF CONTROL AND STATUS I/O

LOW SPEED ELECTRICAL HARDWARE PINS

The timing requirements of the control and status lines are listed in Table 3 of XFP MSA document. They are summarized in the Table below. The 2-wire serial bus timing is described in Chapter 4: XFP 2-Wire Inter-face Protocol in XFP MSA document.

Timing Requirements of Control and Status I/0

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
TX_DIS assert time	t_off		10	tsec	rising edge of TX_DIS to fall of output signal below 10% of nominal
TX_DIS negate time	t_on		2	msec	Falling edge of TX_DIS to rise of output signal above 90% of nominal
Time to initialize	t_init		300	msec	From power on or hot plug after supply meeting Table 4 or from falling edge of P_Down/RST.
Interrupt assert delay	Interrupt_on		200	msec	From occurrence of the condition triggering Interrupt
Interrupt negate delay	Interrupt_off		500	tsec	From clear on read Interrupt flags
P_Down/RST assert delay	P_Down/RST_on		100	tsec	From Power down initiation
Mod_NR assert delay	Mod_nr_on		1	msec	From Occurrence of fault to assertion of MOD_NR
Mod_NR negate delay	Mod_nr_off		1	msec	From clearance of signal to negation of MOD_NR
P-Down reset time		10		tsec	Min length of P-Down assert to initiate reset
RX_LOS assert delay	t_loss_on		100	tsec	From Occurrence of loss of signal to assertion of RX_LOS
RX_LOS negate delay	t_loss_off		100	tsec	From Occurrence of presence of signal to negation of RX_LOS

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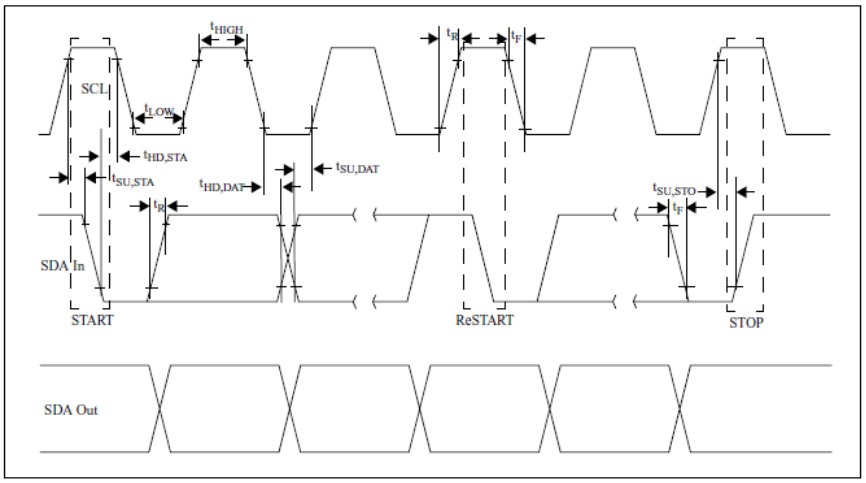
2-WIRE TIMING DIAGRAM AND SPECIFICATIONS

XFP is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. XFP 2-wire bus timing and AC specifications are shown in the following.



Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new trans- mission can start	t_{BUF}	20		µs	Between STOP and START
START Hold Time	$t_{HD,STA}$	0.6		µs	
START Set-up Time	$t_{SU,STA}$	0.6		µs	
Data In Hold Time	$t_{HD,DAT}$	0		µs	
Data In Set-up Time	$t_{SU,DAT}$	0.1		µs	
Input Rise Time (100kHz)	$t_{R,100}$		1000	ns	From $(V_{IL,MAX}$- 0.15) to $(V_{IH,MIN}$ + 0.15)
Input Rise Time (400kHz)	$t_{R,400}$		300	ns	From $(V_{IL,MAX}$- 0.15) to $(V_{IH,MIN}$ + 0.15)
Input Fall Time (100kHz)	$t_{F,100}$		300	ns	From $(V_{IH,MIN}$ + 0.15) to $(V_{IL,MAX}$- 0.15)
Input Fall Time (400kHz)	$t_{F,400}$		300	ns	From $(V_{IH,MIN}$ + 0.15) to $(V_{IL,MAX}$ - 0.15)
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	
Host Supplied Module DeSe- lect Setup Time	Host_select_ setup	2		ms	Setup time on the select lines before start of a host initiated serial bus sequence
Host Supplied Module DeSe- lect Hold Time	Host_select_ hold	10		µs	Delay from completion of a serial bus sequence to changes of transceiver select status
Aborted sequence - bus release	Deselect_ Abort		2	ms	Delay from a host asserting Mod_DeSel (at any point in a bus sequence), to the XFP module releasing SCL and SDA

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