2x5 SFF Dual LC Optical Transceivers

Introduction

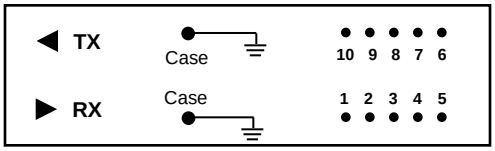
This design guide provides the information needed to incorporate OptixCom's fiber optics transceiver products in the customer's system. This guide will focus on the 2x5 SFF products with single SC connector interface.

The reference guide covers the following topics:

A. Pin Assignment & Description
B. Recommended Interface Circuit
C. Host Board Mechanical Layout
D. Package Outline

A. Pin Assignment & Description

Top View



PIN	Symbol	Description	PIN	Symbol	Description
1	RX GND	Receiver Ground	6	TX Vcc	Transmitter Power Supply
2	RX Vcc	Receiver Power Supply	7	TX GND	Transmitter Ground
3	SD	Signal Detect	8	TX DIS	Transmitter Disable
4	RD–	Receiver Data output –	9	TD+	Transmitter Data Input +
5	RD+	Receiver Data Output +	10	TD–	Transmitter Data Input –

TD+, TD-: DC coupled LVPECL inputs for the transmitter. 50Ω differential lines.

RD+, RD-: Open-emitter out circuits. DC coupled LVPECL outputs for the receiver. 50Ω differential lines.

SD: Signal Detect. Normal optical input levels to the receiver result in a logic "1" output, V_{OH}, asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic "0" output V_{OL}, deasserted. SD is a single-ended LVPECL output and can be terminated with LVPECL techniques via 50 Ω to RX Vcc − 2V.

Alternatively, SD can be loaded with a 180 Ω resistor to RX GND to conserve electrical power with small compromise to signal quality. If SD output is not used, leave it open-circuited. This SD output can be used to drive a LVPECL input on an upstream circuit, such as, SD input or Loss of Signal-bar. Connect to ground if not needed.

TX DIS: Set TTL logic HIGH to turn off the transmitter. TTL logic LOW during normal operation. Open collector compatible. Connect to ground if not needed.

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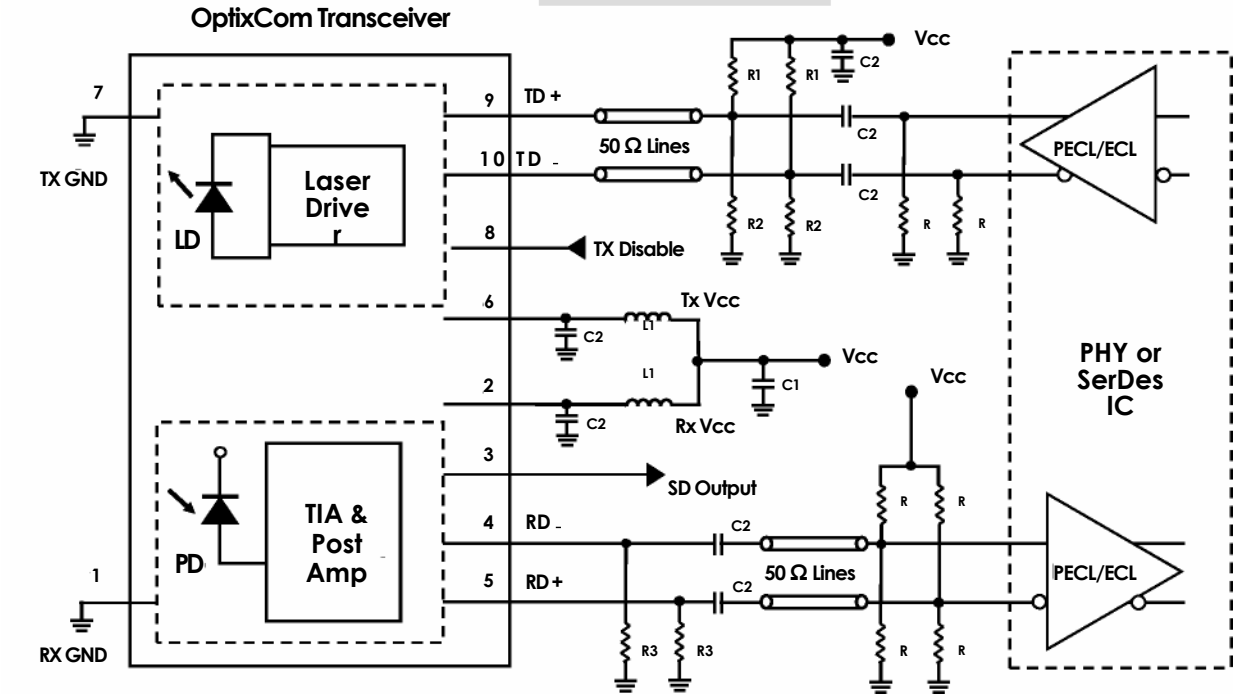
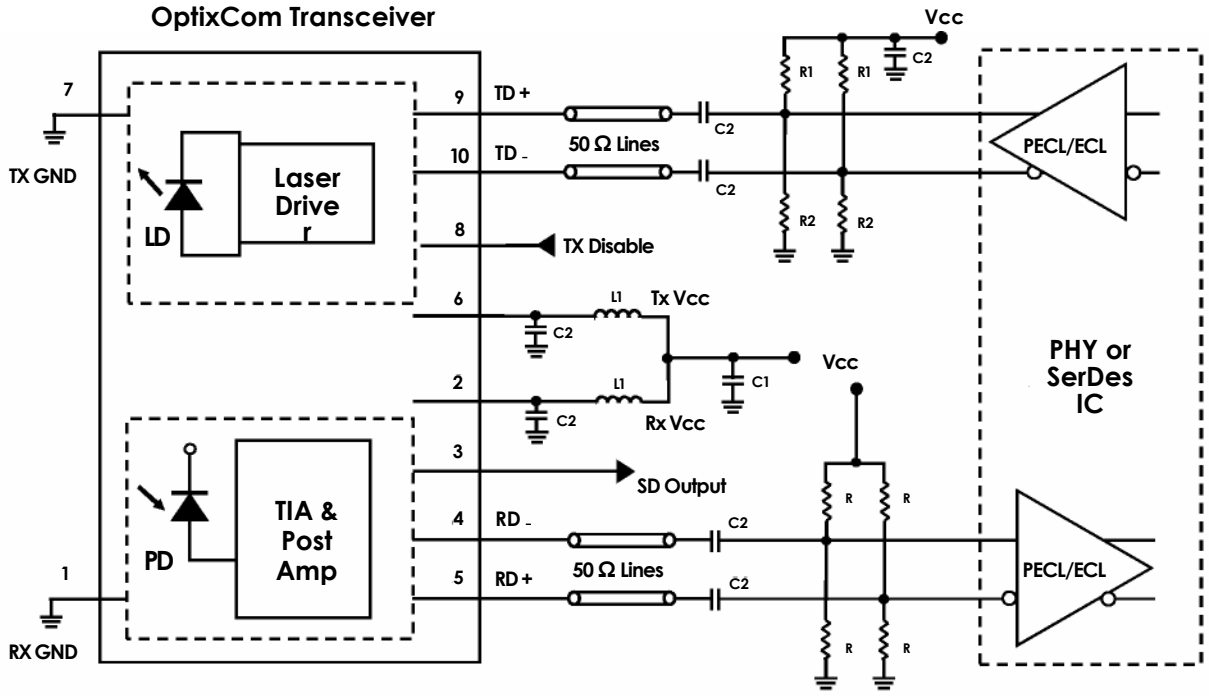
B. Recommended Interface Circuit

DC Coupling I/Os

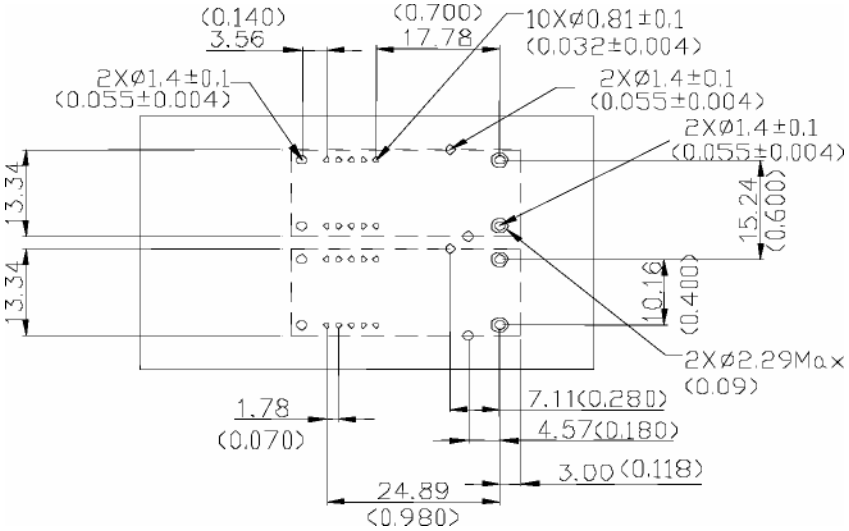


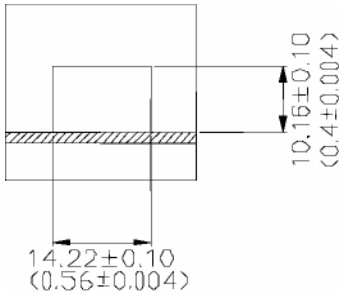
C1: 4.7 µF, C2: 100 nF, L1: 1 µH, R1: 82 Ω, R2: 130 Ω, R3: 180 Ω, R: depends on SerDes IC

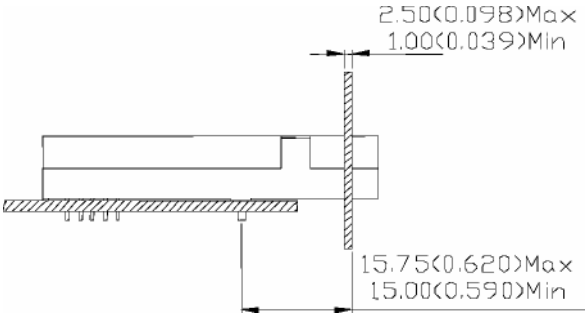
AC Coupling I/Os



C. Host Board Mechanical Layout

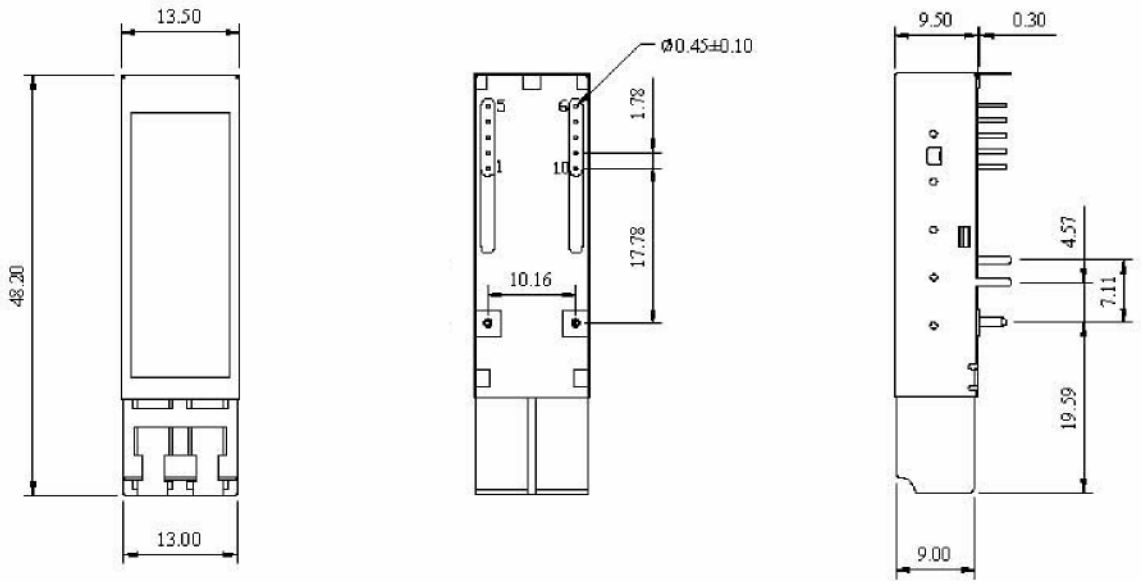


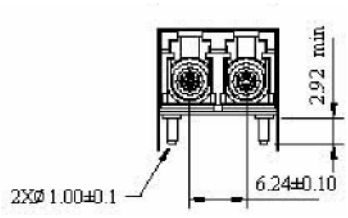


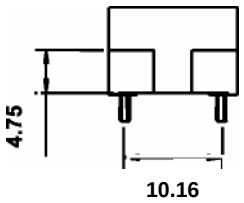


D. Package Outline

Top View **Bottom View** **Side View**







Front View **Rear View**

Unit: mm, typical tolerance for these dimensions is 0.2 mm